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High Speed and Low Power implementation of 3-Weight Pattern Generation Based on Accumulator

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ABSTRACT : The hardware overhead and fault coverage of a circuit is an important problem in integrated circuits and systems. To overcome this problem pseudorandom built-in-self-test (BIST) generators have been widely utilized to test integrated circuits and systems. A Pseudorandom pattern generator (PRPG) is used for generating test patterns (TPG). A weighted Pseudorandom built-in-self-test (BIST) schemes have been utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1, and 0.5 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of BIST pattern generation, as well. The test patterns are generated automatically (ATPG) for a benchmark circuit by using 3-weight pattern generator. So, in this part of project maximum numbers of faults are covered with automatic test pattern generation.

Keywords :- ATPG - Automatic Test Pattern Generation, BIST- Built In Self-Test, CUT - Circuit Under Test, LT RTPG – Low transition Random Test Pattern Generation, LFSR – Linear Feedback Shift Register.

I. INTRODUCTION

Advances in VLSI technology have led to the fabrication of chips that contain a very large number of transistors. The task of testing such a chip to verify correct functionality is extremely complex and often very time consuming. In addition to the problem of testing the chips themselves, the incorporation of the chips into systems has caused test generation's cost to grow exponentially. A widely accepted approach to deal with the testing problem at the chip level is to incorporate Built-In-Self-Test (BIST) capability inside a chip. Built-In-Self-Test (BIST) is the capability of a circuit to test itself. BIST is a design technique in which parts of a circuit are used to test the circuit itself. BIST represents a merger of the concepts of built-in test (BIT) and self-test.This increases the controllability and the observability of the chip, thereby making the test generation and fault detection easier. The test patterns and the expected responses of the circuit under test (CUT) to these test patterns are used by automatic test equipment (ATE) to determine if the actual responses match the expected ones. Ideally, a BIST scheme should be easy to implement and must provide high fault coverage.

A. BIST Techniques

BIST techniques can be classified into two categories, namely **on-line BIST**, which includes concurrent and non-concurrent techniques, and **off-line BIST**, which includes functional and structural approaches, is shown in fig1.2.

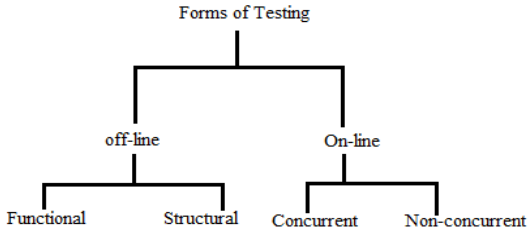

Fig. 1 Forms of testing

B. Test Pattern Generation of Bist

Test pattern generation is the process of defining an effective test set which will drive the circuit under test so that the faults in the circuit. The algorithm used in test pattern generation are usually directed to non-functional testing, which concentrate on propagating any available faults on the circuit nodes to primary outputs. This type of testing is termed fault oriented testing. Test pattern generation is strongly related to fault modelling.

Test pattern generation approaches for BIST schemes can be divided into four categories:

1. Exhaustive testing
2. Pseudorandom testing
   Weighted test generator
   Adaptive test generator

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3. Pseudoexhaustive testing
4. Deterministic testing

II. EXISTING SYSTEM

A. Accumulator cell Design

An Accumulator Cell is designed with Full adder and D-flip flop with set and reset inputs. According to these schemes a typical weight assignment procedure would involve separating the test set into two subsets as follows S1 = {T1,T4} and S2 = {T2,T3}, The weight assignments for these subset is W(S1)={-,-,1,-,1} and W(S2)={-,-,0,1,0}, where a "-" denotes a weight assignment of 0.5, a "1" indicates that the input is constantly driven by the logic "1" value, and "0" indicates that the input is driven by the logic "0" value. The implementation of the weighted-pattern generation scheme is based on the full adder truth table.

1. Operation of Accumulator cell:

A fig 2 shows an accumulator cell with full adder and D-flip flop. In this the upper D-flip flop uses set as reset and reset as set inputs. The output of upper D-flip flop is given as input of full adder. The output of full adder is connected with another d-flip flop with actual set and reset inputs. Full adder uses 3 inputs, 2 inputs from output of both D-flip flops, and another input is Cin. The sum output of full adder is given as input of D-flip flop.

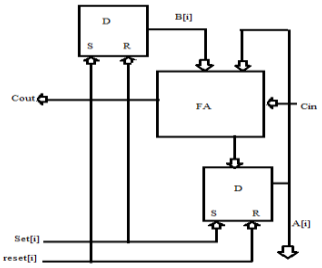

Fig. 2 Accumulator cell

2. Configuration of Accumulator cell:

There are three configurations for Accumulator cell is proposed. The configuration (a) that drives the CUT inputs when A='1' is required. Set[i] = '1' and reset[i] ='0' and hence A='1' and B='0'. Then the output is equal to '1', and Cin is transferred to Cout.

The configuration (b) that drives the CUT inputs when A='0' is required. Set[i] = '0' and reset[i]='1' and hence A='0' and B='1'. Then the output is equal to '0', and Cin is transferred to Cout.

The configuration (c) that drives the CUT inputs when A='-' is required. Set[i]='0' and reset[i]='0'.

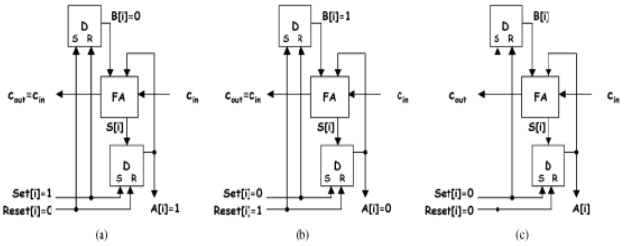

Fig. 3 Configurations of accumulator cell

This condition is also referred as 0.5 weight output or don't care state. The D input of the flip flop of the register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs in order to generate random patterns to the inputs of the CUT.

B. Testing a Circuit by Using Test Vectors

A fig 4 shows a C17 benchmark circuit. In this 5 inputs are used.

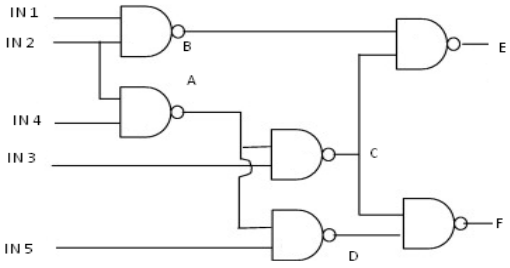

Fig. 4 C17 Benchmark circuit

The weights are applied through set and reset values, the test vectors are generated automatically by pseudorandom method. The fault coverage is calculated. Fig 5 show a C17 benchmark circuit with inputs from accumulator cell output.

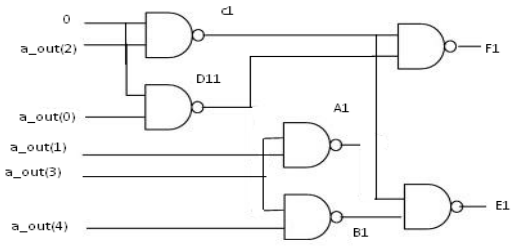

Fig. 5 C17 Benchmark circuit with inputs from accumulator cell output

A benchmark circuit is taken and it is tested by using test vectors which is generated by using pseudorandom pattern generation method. A C17 benchmark circuit is taken and tested by using test vectors. The fault coverage is more by applying these test vectors. These outputs are used as inputs for another benchmark circuit. Stuck-at-

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fault is applied and test vectors are generated automatically

The output of accumulator cell are a_out(0),a_out(1),a_out(2),a_out(3),a_out(4). These outputs are used as inputs for another benchmark circuit. Stuck-at-fault is applied and test vectors are generated automatically. The faults are covered by test vectors. The fault coverage is more by applying these test vectors.

If the fault output is '1' means, it indicates that **"fault is detected"**. If the fault output is '0' means, it indicates that**, "fault is not detected"**. Mostly 90% of faults are detected so, the fault coverage is more.

III. PROPOSED DESIGN

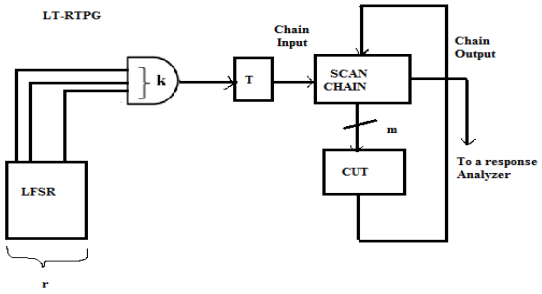

Fig. 6 Architecture of LT-RTPG

The LT-RTPG reduces switching activity during BIST by reducing transition at scan inputs during scan shift operation. An example LT-RTPG is shown in fig.6 . The LT-RTPG is comprised of n -stage LFSR, a K-input AND gate, and a toggle flip flop(T-flip flop). Hence, it can be implemented with very little hardware. Each of K-inputs of the AND gate is connected to either a normal or an inverting output of the LFSR stages. If large K is used, large sets of neighboring state inputs will be assigned identical values in most test patterns, resulting in the decrease fault coverage or the increase in test sequence length. Hence, LT-RTPGs with only K=2 or 3 is used. Since a T-flip flop holds previous values until the input of the T-flip flop is assigned a 1, the same value 'v', where v€{0,1} , is repeatedly scanned into the scan chain until the value at the output of the AND gate becomes 1. Hence, adjacent scan flip flops are assigned identical values in most test patterns and scan inputs have fewer transitions during scan shift operation. Since most switching activity during scan BIST occurs during scan shift operations ,the LT-RTPG can reduce heat dissipation during overall scan testing.

It has been observed that many faults that escape random patterns are highly correlated with each other and can be detected by continuously complementing values of a few inputs from a parent test vector. This is a low hardware overhead of TPG for scan based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with a reasonable length of test sequence.

Since the correlation between consecutive vectors applied to a circuit during BIST is significantly lower, switching activity in the circuit can be significantly higher during BIST than that during its normal operation.

Excessive switching activity during test application can damage CUTs during BIST. The LT-RTPG reduces switching activity during BIST by reducing transition at scan inputs during scan shift operations.

IV. SIMULATION RESULTS

A. Simulation Result For Accumulator Cell

The waveform of Accumulator cell is shown in the fig 7.

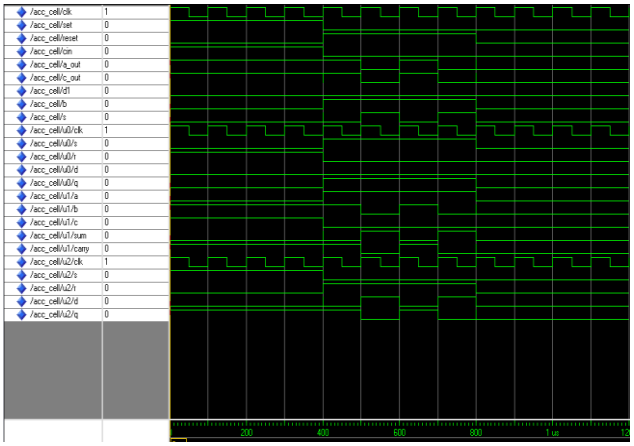

Fig. 7 Waveform of Accumulator cell

B. Simulation Result for Accumulator cell Configurations

The waveform of Accumulator cell's configurations is shown in the fig 8. The configuration (a) that drives the CUT inputs when A='1' is required. Set[i] = '1' and reset[i] ='0' and hence A='1' and B='0'. Then the output is equal to '1', and Cin is transferred to Cout.

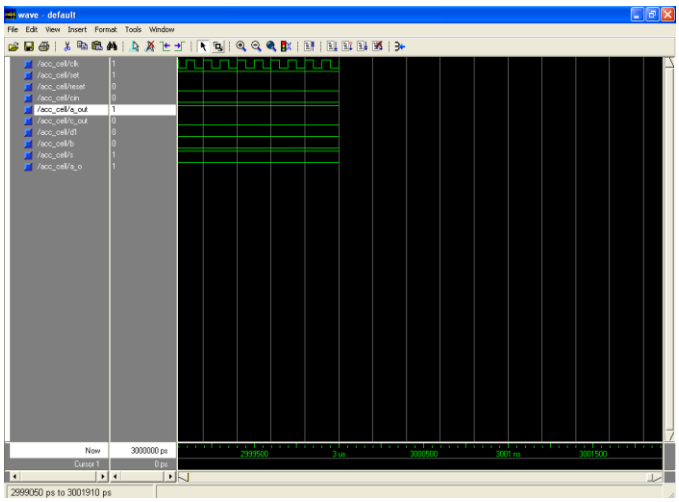

Fig 8. Waveform for the configuration of set='1' and reset='0'

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The waveform for Accumulator cell with set='0' and reset='1' is shown in the Fig. 9.

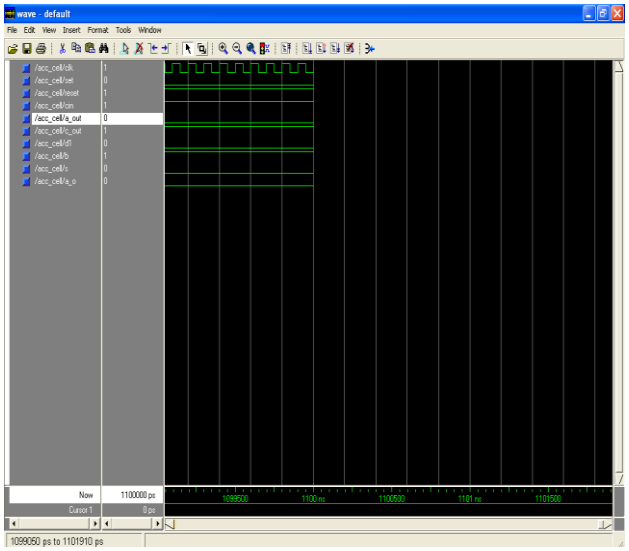

Fig. 9 waveform of the configuration of set='0' and reset='1'

The waveform for Accumulator cell with set='0' and reset='0' is given in fig 10.

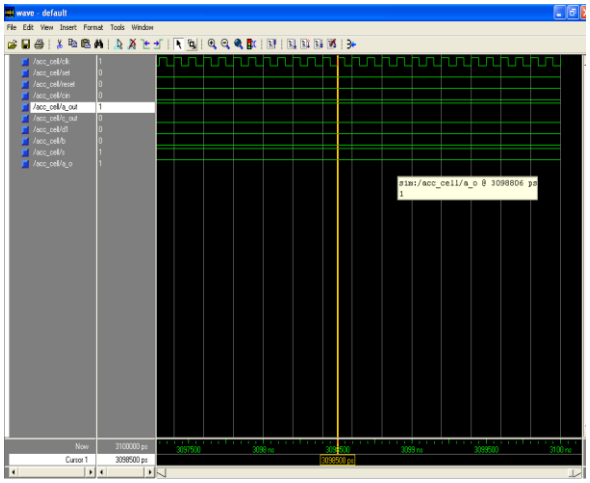

Fig. 10 Waveform of the configuration of set='0' and reset='0'

1. Simulation Result for Test Vector Generation for Fault Coverage:

Fig 11 shows the applied test vectors for set and reset are "10000" and "10001" respectively. If fault is present means fault output parameter is set as'1'. If no fault in circuit means, fault will be set as '0'. For this applied test vectors the test patterns are generated automatically.

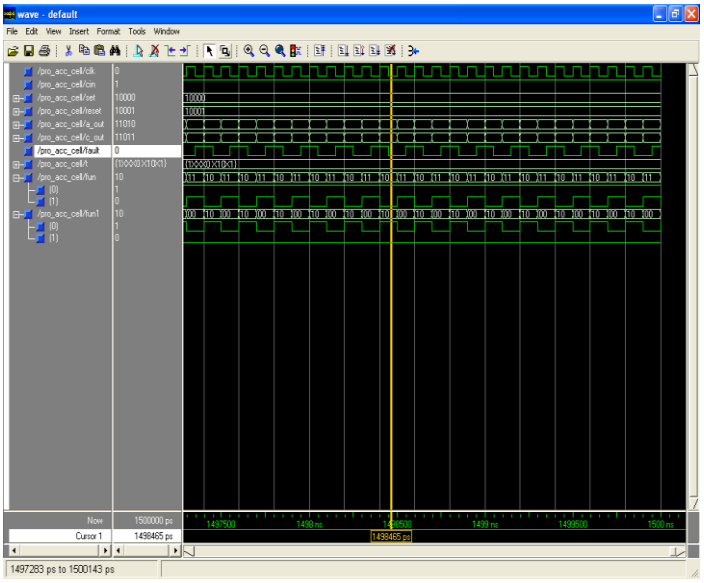

Fig. 11 Output Waveform For Benchmark Circuit Using Accumulator Cell

In fig 12 the applied test vectors for set and reset are "10000" and "10111" respectively. If fault is present means fault output parameter is set as'1'. If no fault in circuit means, fault will be set as '0'. For this applied test vectors the test patterns are generated automatically. In this, the fault coverage is more compared to previous applied test vectors.

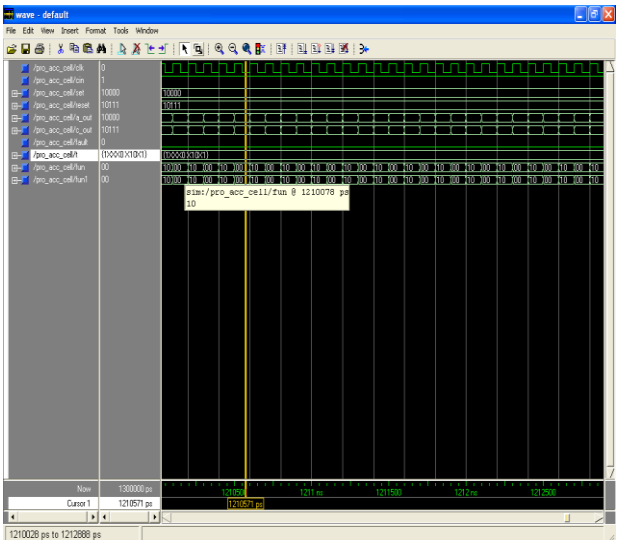

Fig. 12 Output Waveform For Benchmark Circuit Using Accumulator Cell

2. Simulation Result for LT-RTPG

The waveform for LT-RTPG is shown in Fig. 13

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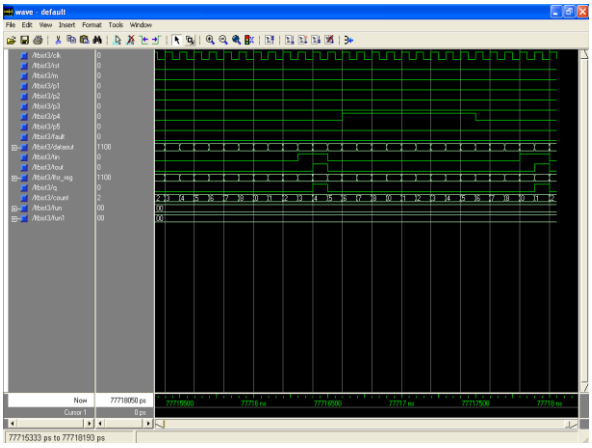

Fig. 13 Waveform of LT-RTPG for Fault not detected

The waveform for LT-RTPG with fault detected is shown in Fig. 14

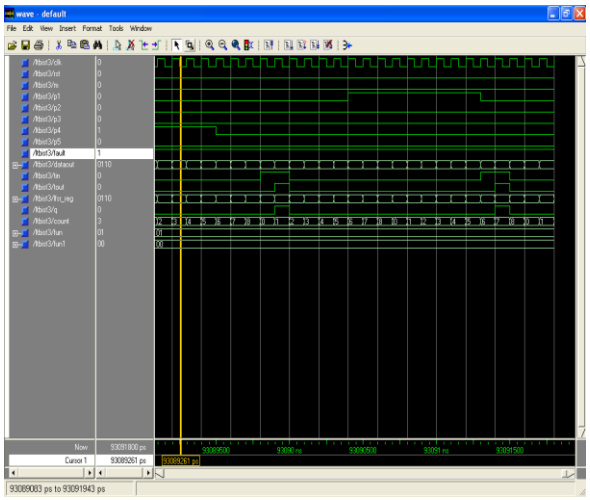

Fig. 14 Waveform of LT-RTPG for Fault detected

V. POWER TABLE

SERIES	Accumulator	LT-RTPG	WR-BIST
POWER[W]	0.08	0.025	0.024
Fault coverage[%]	50	75	100

A. Power Comparison Chart

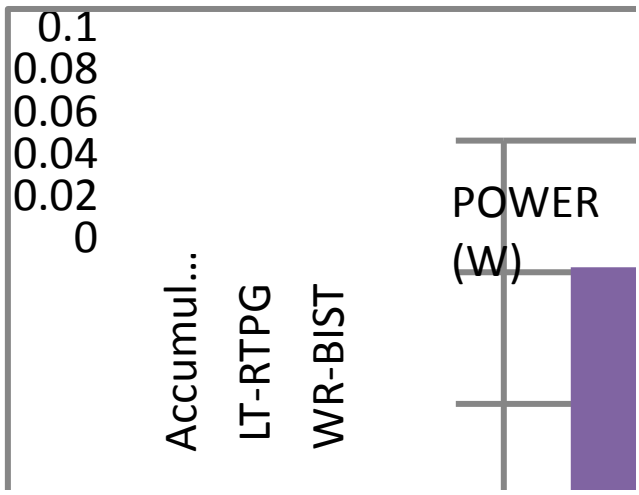

Fig. 8 Power Comparison Chart

VI. CONCLUSION

An Accumulator-based 3-weight technique can reduce the hardware implementation cost and fault coverage is more. The power is get reduced and increased fault coverage. The fault coverage is more and it is proved by testing a c17 benchmark circuit. The time for testing a circuit is more and very simple method, because of its automatic test pattern generation. The test patterns are generated automatically for applied test vectors

From I can conclude that scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations, thus the LT-RTPG can reduces the switching activity during overall scan testing

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